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## DAFTAR PUSTAKA

- [1] U. Saravanakumar, K. Rajasekar dan R. Rangarajan, "Implementation of Scheduling Algorithms for On Chip Communications," *International Journal of Computer Applications*, vol. 62, no. 14, January 2013.
- [2] B. A. Abderazek, "Network-on-Chip for Multi- and Many-Core Systems," dalam *Multicore Systems On-Chip*, New York, Springer Science & Business Media, 2010, p. 35.
- [3] R. Marculescu, U. Y. Ogras, L.-S. Peh, N. E. Jerger dan Y. Hoskote, "Outstanding Research Problems in NoC Design: System, Microarchitecture, and Circuit Perspectives," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 1, pp. 3-21, 2009.
- [4] F. Lokananta, "Network-on-Chip Communication Architecture Design, Analysis, Optimization, and Evaluation in a Multi-Processor System-on-Chip," M.S. thesis, 2015.
- [5] Y. Liu, J. Jin dan Z. Lai, "A dynamic adaptive arbiter for Network-on-Chip," *Journal of Microelectronics, Electronic Components and Materials*, vol. 43, no. 2, pp. 111-118, 2013.
- [6] M. M. Lee, J. Kim, D. Abts, M. Marty dan J. W. Lee, "Probabilistic Distance-based Arbitration: Providing Equality of Service for Many-core CMPs,"

*Proceedings of the 2010 43rd Annual IEEE/ACM International Symposium on Microarchitecture*, pp. 509-519, 2010.

- [7] D. Abts dan D. Weisser, "Age-Based Packet Arbitration in Large-Radix k-ary n-cubes," dalam *Proceedings of the 2007 ACM/IEEE Conference on Supercomputing*, Reno, 2007.
- [8] F. A. Samman, T. Hollstein dan M. Glesner, "Adaptive and Deadlock-Free Tree-Based Multicast Routing for Networks-on-Chip," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no. 7, pp. 1067-1080, 2010.
- [9] M. Modarressi, A. Tavakkol dan H. Sarbazi-Azad, "Application-Aware Topology Reconfiguration for On-Chip Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 19, no. 11, pp. 2010-2022, 2011.
- [10] M. M. Kim, J. D. Davis, M. Oskin dan T. Austin, "Polymorphic On-Chip Networks," *Proceedings of the 35th Annual International Symposium on Computer Architecture*, vol. 36, no. 3, pp. 101-112, 2008.
- [11] Accellera, "Universal Verification Methodology (UVM) 1.1 User's Guide," 18 May 2011. [Online]. Available: [http://accellera.org/images/downloads/standards/uvm/uvm\\_users\\_guide\\_1.1.pdf](http://accellera.org/images/downloads/standards/uvm/uvm_users_guide_1.1.pdf). [Diakses 10 September 2016].

- [12] Hong Kong University of Science and Technology, “MCSL Network-on-Chip Traffic Suite,” January 2014. [Online]. Available: <http://www.ece.ust.hk/~eexu/>. [Diakses 2 July 2017].
- [13] T. C. Xu, A. W. Yin, P. Liljeberg dan H. Tenhunen, “An Analysis of Designing 2D/3D Chip Multiprocessor with Different Cache Architecture,” dalam *NORCHIP*, Tampere, 2010.
- [14] S. T. Nguyen dan S. Oyanagi, “An Improvement of Router Throughput for On-Chip Networks Using On-the-fly Virtual Channel Allocation,” [Online]. Available: [https://www.researchgate.net/publication/220826922\\_An\\_Improvement\\_of\\_Router\\_Throughput\\_for\\_On-Chip\\_Networks\\_Using\\_On-the-fly\\_Virtual\\_Channel\\_Allocation](https://www.researchgate.net/publication/220826922_An_Improvement_of_Router_Throughput_for_On-Chip_Networks_Using_On-the-fly_Virtual_Channel_Allocation). [Diakses 8 July 2017].
- [15] W. Liu, J. Xu, X. Wu, Y. Ye, X. Wang, W. Zhang, M. Nikdast dan Z. Wang, “A NoC Traffic Suite Based on Real Applications,” dalam *2011 IEEE Computer Society Annual Symposium on VLSI*, Chennai, 2011.

